# AND8381/D

# SOT-963 527AD Dual MOSFET Package Board Level Application and Thermal Performance

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**APPLICATION NOTE**

## INTRODUCTION

ON Semiconductor dual small signal MOSFETs offered in the ultra−small SOT−963 527AD package are optimized for power management in space−constrained portable electronics. The package exhibits a 30% smaller mount area than comparable MOSFET solutions offered in a single SOT−723 package and a 60% smaller footprint than SOT−563 devices.

This technical note discusses the SOT−963 527AD package overview, pad pattern, evaluation board layout and thermal performance.

## PACKAGE OVERVIEW

Figure 1 illustrates a dual site SOT−963 527AD semiconductor device package and pin−out description. This 1 mm x 0.8 mm package features short legs which reduce the thermal path to an external heatsink/pcb. Also, the low vertical clearance (< 0.5 mm) allows for an easy fit in extremely thin environments. The efficient and compact design of this package promotes increased thermal dissipation and reduced electrical parasitics.

1

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

**Figure 1. SOT−963 527AD**

## PAD PATTERN

A recommended solder−mask defined mounting footprint is defined in Figure 2. Increased thermal dissipation is promoted by adding vias to other pcb layers. An evaluation board containing the minimum recommended pad pattern and aforementioned vias is shown in Figure 3 of the subsequent section.

Mounting the device on a pcb requires careful attention toward soldering techniques. Negligent soldering practices may result in a short circuit due to the formation of a conducting bridge across the minuscule distance (0.15 mm) between pins.

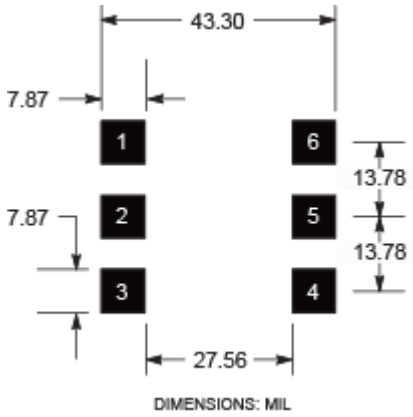


**Figure 2. Minimum Recommended Pad Pattern**

## EVALUATION BOARD

The evaluation board, shown in Figure 3, measures 0.6 in by 0.5 in. The board contains 1.0 oz copper thickness on top−side and 1.0 oz copper thickness on the underside. Vias are added through to the underside of the board where contact is made with a copper pad area of approximately 0.198 square inch. On top−side, the copper pad areas surrounding the two drain leads are each increased to approximately 0.031 square inch for a total dissipation path area of 0.229 square inch per drain.



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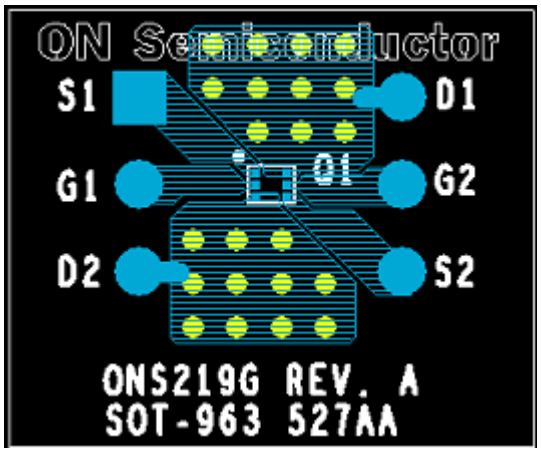
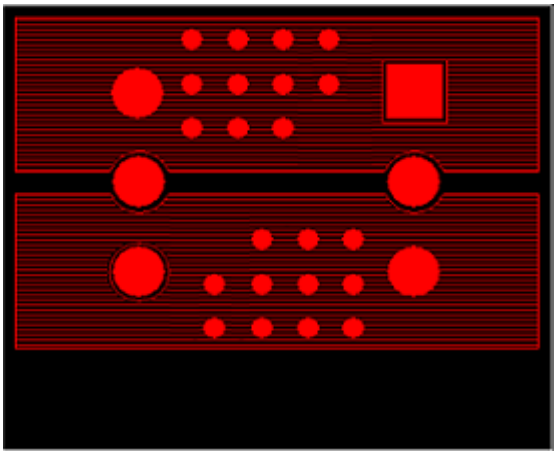



Front of Board



Back of Board

**Figure 3. Evaluation Board**

This 6−pin DIP design allows the use of sockets which facilitates wire interfacing. Figure 4 represents a SOT−963 527AA package mounted on the evaluation board with and without test pins. A quick thermal analysis of this board is conducted by inducing a saturation current of 829 mA. This yields a junction temperature of 143.0°C and a board temperature of 53.9°C. Figure 5 shows a thermal image of this board under the aforementioned conditions.

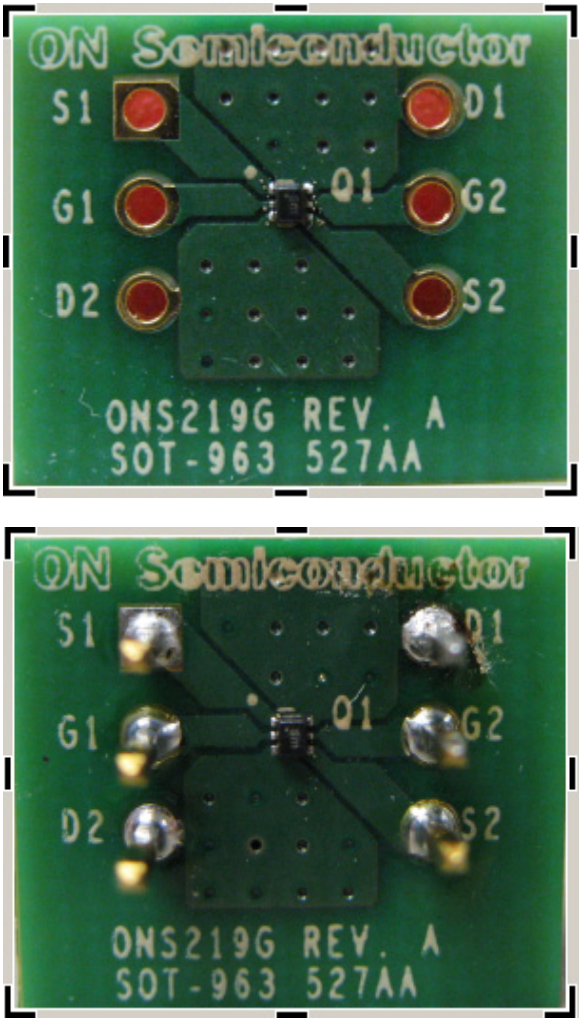



**Figure 4. Mounted Device**

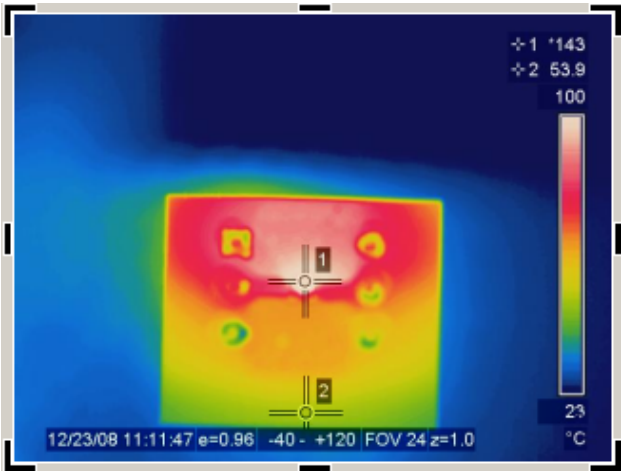



**Figure 5. Thermal Image of Mounted Device**

Further results from the measured thermal performance of this package are described in the subsequent section. Testing included a thermal analysis of the package surface mounted on a FR4 board using the minimum recommended pad size.

## THERMAL PERFORMANCE

### Assumptions and Definitions

The subsequent sections outline the thermal performance of a SOT−963 527AD. All values and equations are obtained from simulations and pertain to the Theta(DC) matrix with both MOSFETs operating at maximum power unless otherwise specified. A 10% duty cycle is arbitrarily chosen to evaluate various thermal responses. Refer to Figure 10 for thermal responses at different duty cycles. The simulation models used to derive the results in this section are modeled around results obtained from physical testing and are considered reliable. Table 1 defines a set of parameters used throughout this section.

**Table 1. THERMAL ANALYSIS PARAMETERS**

| Symbol | Definition |
|---|---|
| $T_{Jn}$ | Junction Temperature of MOSFET “n” |
| $T_A$ | Ambient Temperature |
| $P_{Dn}$ | Power Dissipation of MOSFET “n” |
| $P_{TOTAL}$ | Total Power Dissipation |
| $R_{\theta-JnL}$ | Thermal Resistance from Junction “n” to Location ”L” |
| $R(u)_{EFF}$ | Effective (maximum) Thermal Resistance of Package |
| $\Psi_{Fn-L}$ | Thermal Reference between Foot ”n” and location ”L” |
| $\Psi_{Jn-L}$ | Thermal Reference between Junction “n” and location ”L” |

The number designation associated with “foot” in the subscript of each Ψ (read psi) term corresponds to the pin identification number as shown in Figure 6.

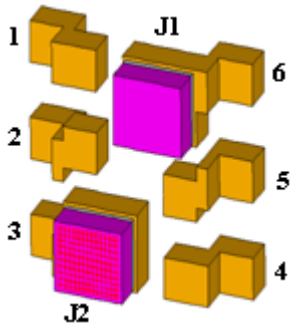



**Figure 6. Foot and Junction Identification**

Figures 7 and 8 represent Cauer and Foster Ladders respectively. This technical note assumes the reader has a general understanding of these networks. Please refer to the documentation cited under references for detailed descriptions of thermal RC networks. In this section, the Foster network is used to calculate various thermal characteristics. For example, as seen in Figure 8, a particular thermal resistance occurs between the junction and C1/C2 node (denoted here as $\Psi_{Jn-L}$). Then, the sum of all thermal references between the C1/C2 node and the Cn−1/Cn node is called a junction−to−foot thermal *reference* ($\Psi_{Jn-Fn}$). Therefore, in the case of Figure 8, the junction−to−ambient thermal *resistance* ($R_{\theta JnA}$) is measured as the sum of thermal references such that;

$$R_{\theta JnA} = \Psi_{Jn-Fn} + \Psi_{Fn-A} \qquad \text{(eq. 1)}$$

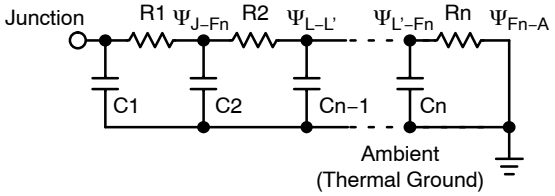



**Figure 7. Grounded Capacitor Thermal Network (“Cauer” Ladder)**

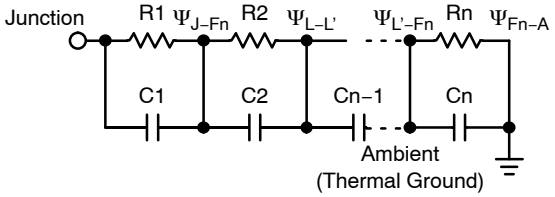



**Figure 8. Non−Grounded Capacitor Thermal Network (“Foster” Ladder)**

### Junction−to−Foot / Foot−to−Ambient

The Foster Network junction−to−foot thermal references and foot−to−ambient thermal references under steady state conditions at $T_A$ = 25°C are outlined in Table 2. The values below are derived using J1 as an initial reference. It is important to note that using J2 as an initial reference yields different values for the psi terms in Table 2 but the thermal resistance value does not change.

**Table 2. THERMAL REFERENCE PARAMETERS**

| 10% Duty Cycle | Junction−to−Foot | |
|---|---|---|
| $P_{D1} = P_{D2}$ | 0.175 mW | 0.210 mW |
| Copper Area | 100 mm² (1 oz) | 500 mm² (1 oz) |
| $\Psi_{J1-F3}$ | 369.4°C/W | 346.8°C/W |
| $\Psi_{J1-F6}$ | 231.7°C/W | 241.7°C/W |
| **10% Duty Cycle** | **Foot−to−Ambient** | |
| $P_{D1} = P_{D2}$ | 0.175 mW | 0.210 mW |
| Copper Area | 100 mm² (1 oz) | 500 mm² (1 oz) |
| $\Psi_{F3-A}$ | 159.0°C/W | 105.8°C/W |
| $\Psi_{F6-A}$ | 296.7°C/W | 210.9°C/W |

A relationship for the thermal resistance of each device is established by using either of the following relationships,

$$R_{\theta J1A} = \Psi_{J1-F3} + \Psi_{F3-A} \quad \text{(eq. 2)}$$

$$R_{\theta J1A} = \Psi_{J1-F6} + \Psi_{F6-A} \quad \text{(eq. 3)}$$

Substituting appropriate values, from Table 2, into the above equations yields $R_{\theta J1A} = R_{\theta J2A} = 528.4°C/W$ for the FR−4 at 100 $mm^2$ and $R_{\theta J1A} = R_{\theta J2A} = 452.6°C/W$ for FR−4 at 500 $mm^2$ min pad size. In both cases the thermal resistances of each device are directly proportional to each other due to symmetrical die sizes.

### Junction−to−Ambient

The thermal response of this package is parameterized by thermal interactions between adjacent MOSFETS. Switching one device OFF, such as Q1, alters the junction temperature and thermal resistance of each FET. Heat from Q2 will transfer to Q1 causing Q1 to exhibit an added thermal resistance equivalent to a factor of $\Psi_{Q1Q2}$. The following matrix equation illustrates the aforementioned relationships for a junction−to−ambient thermal response;

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta J1A} & \Psi_{Q1Q2} \\ \Psi_{Q2Q1} & R_{\theta J2A} \end{bmatrix} \begin{Bmatrix} P_{D1} \\ P_{D2} \end{Bmatrix} + T_A \quad \text{(eq. 4)}$$

Using data from Table 3, this matrix allows various junction temperatures and, in turn, the package $R(u)_{EFF}$ to be calculated at assumed ambient temperatures. $R(u)_{EFF}$ is defined as,

$$R_{(u)EFF} = \left[T_{MAX} - T_A\right] / P_{TOTAL} \quad \text{(eq. 5)}$$

Where $R(u)_{EFF}$ is a function of either direct current or a transient response and $T_{MAX}$ is the maximum junction temperature between $T_{J1}$ and $T_{J2}$. Table 3 outlines the junction−to−ambient thermal analysis of this package, using J1 as the initial reference. Notice that $R_{\theta J1A} = R_{\theta J2A}$ and $\Psi_{Q1Q2} = \Psi_{Q2Q1}$ due to symmetrical die sizes. Furthermore, Quick reference steady state matrices are located in the Appendix.

**Table 3. JUNCTION−TO−AMBIENT THERMAL RESPONSE**

| 10% Duty Cycle | Steady State | | Pulsed time = 5 sec |
|---|---|---|---|
| Copper area | 100 $mm^2$ (1 oz) | 500 $mm^2$ (1 oz) | 100 $mm^2$ (1 oz) |
| $P_{D1} = P_{D2}$ | 175 mW | 210 mW | 175 mW |
| $T_{AMB}$ | 25.0°C | 25.0°C | 25.0°C |
| $R_{\theta-JA}$ | 528.4°C/W | 452.6°C/W | 528.4°C/W |
| $R(t)_{\theta-JA}$ | | | 366.9°C/W* |
| $\Psi_{Q1Q2} = \Psi_{Q2Q1}$ | 198.5°C/W | 146.7°C/W | 67.3°C/W* |
| $T_{J1}$ | 152.2°C | 151.0°C | 152.2°C |
| $T_{J2}$ | | | |
| $T_J$ (t) | | | 101.0°C* |
| $R(DC)_{EFF}$ | 363.0°C/W | 300.0°C/W | 363.0°C/W |
| $R(t)_{EFF}$ | | | 217.0°C/W |

*Refer to Appendix−A for Theta(t) matrix equations.

### Junction−to−Board

A matrix equation yielding junction temperatures for assumed board temperatures is defined by equation 6,

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} \left(R_{\theta J1A} - \Psi_{B-A}\right) & \left(\Psi_{Q1Q2} - \Psi_{B-A}\right) \\ \left(\Psi_{Q2Q1} - \Psi_{B-A}\right) & \left(R_{\theta JA1} - \Psi_{B-A}\right) \end{bmatrix} \begin{Bmatrix} P_{D1} \\ P_{D2} \end{Bmatrix} + T_{BOARD} \quad \text{(eq. 6)}$$

Where $\Psi_{B-A}$ is the thermal reference from board−to−ambient. Values for $R_{\theta JA}$ and $\Psi_{Q1Q2}$ are defined in Table 3. Table 4 outlines the junction−to−board thermal analysis of this package surface mounted on an FR4 board. Furthermore, Quick reference steady state matrices are located in the Appendix.

**Table 4. JUNCTION−TO−BOARD THERMAL RESPONSE**

| 10% Duty Cycle | Steady State | | Pulsed time = 5 sec |
|---|---|---|---|
| Cu area | 100 mm$^2$ [1 oz] | 500 mm$^2$ [1 oz] | 100 mm$^2$ [1 oz] |
| $P_{D1} = P_{D2}$ | 175 mW | 210 mW | 175 mW |
| $T_{AMB}$ | 25.0°C | 25.0°C | 25.0°C |
| $\Psi(t)_{B-A}$ | 199.1°C | 143.7°C | 67.4°C* |
| $T_{J1} = T_{J2}$ | 152.0°C | 151.0°C | 152.0°C* |
| $T_{J1}(t) = T_{J2}(t)$ | | | 101.0°C |
| $T_{BOARD}$ (DC) | 95.0°C | 85.0°C | 95.0°C |
| $T_{BOARD}$ (t) | | | 49.0°C |
| $R(DC)_{EFF-BOARD}$ | 199.0°C/W | 144.0°C/W | 199.0°C/W |
| $R(t)_{EFF-BOARD}$ | | | 67.0°C/W |

*Refer to Appendix−A for Theta(t) matrix equations.

## SUMMARY

Figure 9 illustrates a steady state plot of the change in thermal resistance and max power dissipation that occurs with a change in the amount of copper spread across a given area. Figure 10 illustrates the packages change in junction−to−ambient thermal resistance with respect to pulse time. Evaluating these plots by inspection yields the following maximum values;

**Table 5. MAXIMUM RATINGS**

| Cu Area | $R_{\theta J1A}$ | Max Power |
|---|---|---|
| 100 mm$^2$ [1 oz] | 528.4°C/W | 0.237 W |
| 500 mm$^2$ [1 oz] | 452.6°C/W | 0.276 W |

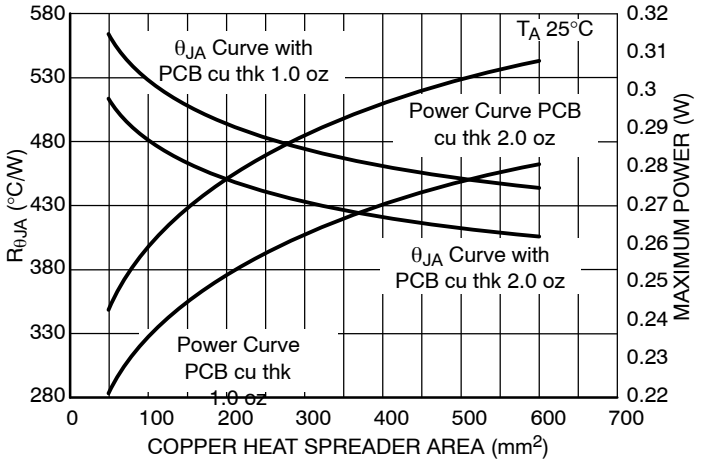



**Figure 9. Self−Heating Thermal Characteristics as a Function of Copper Area on the PCB**

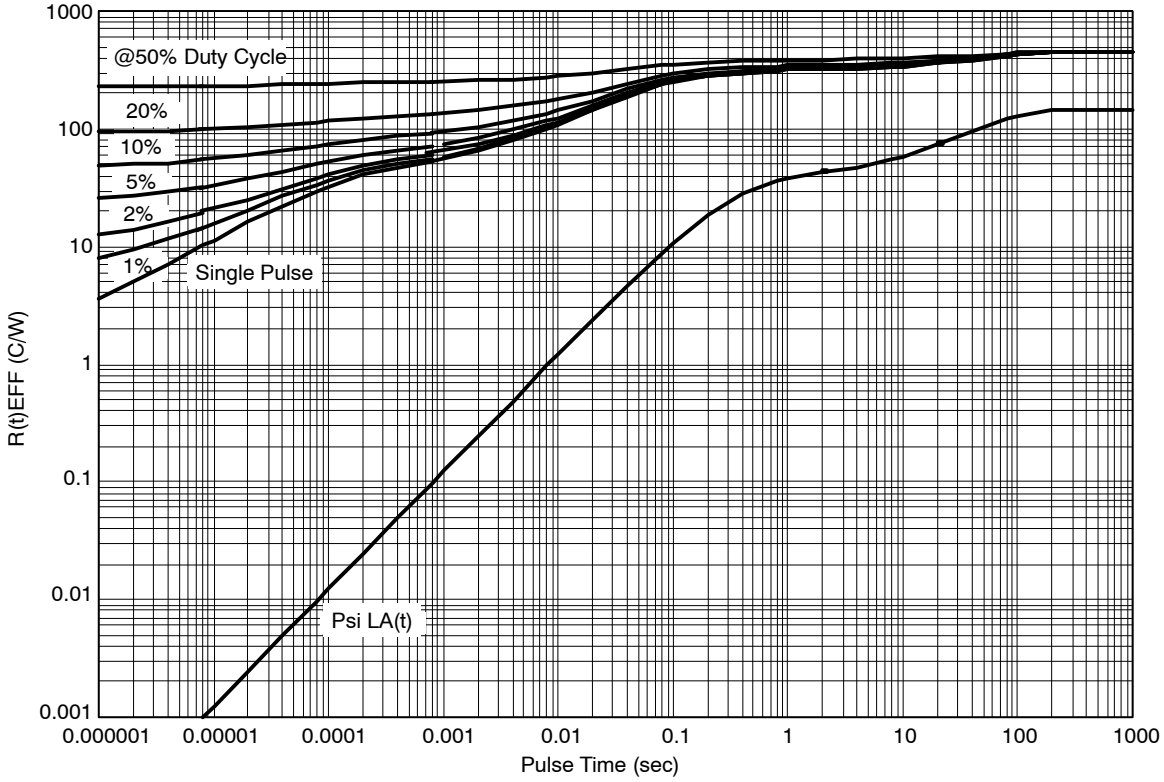



**Figure 10. Thermal Response**

**References**

1. R.P. Stout, D.T. Billings, “How to Extend a Thermal−RC−Network Model (Derived From Experimental Data) to Respond to an Arbitrarily Fast Input,” *ON Semiconductor*, 2006.
2. R.P. Stout, “Thermal RC Ladder Networks; Packaging Technology Development ,” *ON Semiconductor*, 2006.
3. R.P. Stout, “General Thermal Transient RC Networks,” *ON Semiconductor*, 2006.

## APPENDIX

**Steady State Junction−to−Ambient Quick Reference Matrix (1 oz. Cu), 10% DC.**

**FR−4 at 100 mm²**

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} 528.4 & 198.5 \\ 198.5 & 528.4 \end{bmatrix} \begin{Bmatrix} 0.175 \\ 0.175 \end{Bmatrix} + T_A$$

**FR−4 at 500 mm²**

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} 452.6 & 146.7 \\ 146.7 & 452.6 \end{bmatrix} \begin{Bmatrix} 0.21 \\ 0.21 \end{Bmatrix} + T_A$$

**Steady State Junction−to−Board Quick Reference Matrix (1 oz. Cu), 10% DC.**

**FR−4 at 100 mm²**

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} 329.3 & -0.6 \\ -0.6 & 329.3 \end{bmatrix} \begin{Bmatrix} 0.175 \\ 0.175 \end{Bmatrix} + T_{BOARD}$$

**FR−4 at 500 mm²**

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} 308.9 & 3.0 \\ 3.0 & 308.9 \end{bmatrix} \begin{Bmatrix} 0.21 \\ 0.21 \end{Bmatrix} + T_{BOARD}$$

**Junction−to−Ambient Theta(t) Matrix Equations**

$$\Psi'_{QXQY} = \sum_{n=1}^{m} \Psi(\tau_n)_{J-A} \times \left[1 - \exp\left(-t_{pulse}/\tau_n\right)\right] \quad \text{(eq. 7)}$$

$$R'_{\theta J1A} = \sum_{n=1}^{m} \Psi(\tau_n)_{\theta J1A} \times \left[1 - \exp\left(-t_{pulse}/\tau_n\right)\right] \quad \text{(eq. 8)}$$

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} \begin{bmatrix} R'_{\theta J1A} & \Psi'_{Q1Q2} \\ \Psi'_{Q2Q1} & R'_{\theta J1A} \end{bmatrix} \begin{Bmatrix} P_{D1} \\ P_{D2} \end{Bmatrix} + T_A \quad \text{(eq. 9)}$$

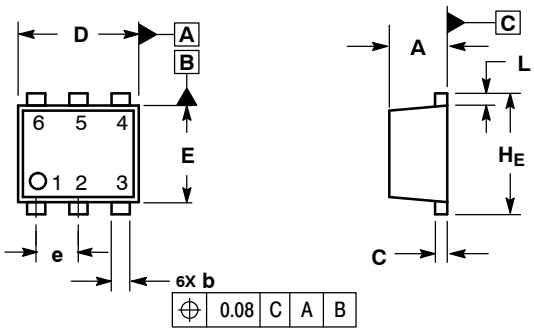
**Junction−to−Board Theta(t) Matrix Equations**

$$\Psi'_{B-A} = \sum_{n=1}^{m} \Psi(\tau_n)_{B-A} \times \left[1 - \exp\left(-t_{pulse}/\tau_n\right)\right] \quad \text{(eq. 10)}$$

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} \left(R'_{\theta J1A} - \Psi'_{B-A}\right) & \left(\Psi'_{Q1Q2} - \Psi'_{B-A}\right) \\ \left(\Psi'_{Q2Q1} - \Psi'_{B-A}\right) & \left(R'_{\theta J1A} - \Psi'_{B-A}\right) \end{bmatrix} \begin{Bmatrix} P_{D1} \\ P_{D2} \end{Bmatrix} + T_{BOARD} \quad \text{(eq. 11)}$$

## PACKAGE DIMENSIONS

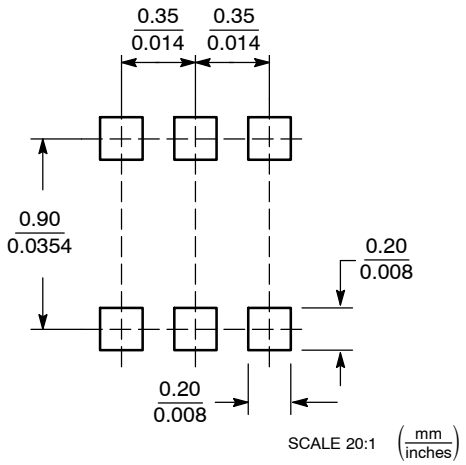
**SOT−963**
CASE 527AD−01
ISSUE D




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.34 | 0.37 | 0.40 | | | |
| b | 0.10 | 0.15 | 0.20 | 0.004 | 0.006 | 0.008 |
| C | 0.07 | 0.12 | 0.17 | 0.003 | 0.005 | 0.007 |
| D | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| E | 0.75 | 0.80 | 0.85 | 0.03 | 0.032 | 0.034 |
| e | 0.35 BSC | | | 0.014 BSC | | |
| L | 0.05 | 0.10 | 0.15 | 0.002 | 0.004 | 0.006 |
| $H_E$ | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |

## SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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